16.6 An Integrated Magnetic Sensor with Two Continuous-Time ΔΣ-Converters and Stress Compensation Capability

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Accurate magnetic sensors with digital signal processing and means for individual adjustment are required for many automotive and industrial applications. Previous magnetic sensors have used separate choppers, preamps, anti-aliasing filters and switched capacitor converters, but the compact magnetic sensor presented here combines the spinning-current Hall probe and a chopped 3rd-order continuous-time ΔΣ-converter (CT-ΔΣ–ADC) with multibit feedback to optimize noise and EMI performance at minimum chip area and power (Fig 16.6.1). The improved architecture of the CT-ADC includes an additional digital tracking loop and range switching in the feedback DAC (Fig. 16.6.2) to increase the robustness and the DR to 90dB in a bandwidth of 4kHz.

Low offset drift of 50μT or 5μV input-referred offset at f_{chop} = 32kHz is achieved in the automotive temperature range from -50 to 150°C. Instead of adjusting the resistors or capacitors in the CT-ΔΣ loops for stability, a new bandgap-based method compensates the technology spread (25%) and temperature coefficient between the *RC* time constants of these loops and the ADC clock frequency f_{ADC} derived from an *RC*-relaxation oscillator to <7%, (Fig. 16.6.2).

A second chopped CT-ΔΣ-ADC delivers a temperature signal to enable digital 3rd-order compensation of the Hall sensitivity (Fig. 16.6.1) instead of traditional analog compensation. With multiplexed operation, this 2nd ADC converts a mechanical stress signal for compensating the package-induced long-term drift of the magnetic sensitivity digitally. A new bandgap-based piezoresistive stress sensor acquires the dominant components of the stress tensor.

The feedback structure of the Hall-CT-ΔΣ-ADC includes an inherent low-pass filter rejecting disturbances from the chopper and the mismatch-shaped multibit DAC. In addition, it has low noise because no alias effects appear in the CT-signal path (Fig. 16.6.2). Although, traditionally, 2^n-1 comparators are required to drive an n-bit feedback DAC, here only two comparators are used to save area and current. They provide a signal for a simple three-level inner-loop feedback signal and a signal for an additional up/down counter. The up/down counter performs digital tracking to implement a 5b outer-loop and therefore an increased DR. Bypassing this loop with a signal of the same weight ensures its stability. The DR is further increased by 12dB with range switching of the feedback DAC in the outer loop and switching the capacitors in the first integrator.

Common two-stage differential G_m-*C* integrators are used with capacitors in the feedback path of the CT-ΔΣ-ADC to prevent leakage currents and parasitic capacitors from affecting the transfer function. Current feedback to the source-degenerated input pair of the first stage is implemented as in [2] to provide a very accurate transconductance G_{m1} (Fig. 16.6.3). The load resistors of the first stage are replaced by current sources to increase the gain. All current sources of the first stage are source-degenerated to reduce the noise. Although the second stage is only a 1-stage transconductance instead of an opamp, this architecture also provides an accurate transconductance; $G_{m1} = 1/R_{sense}$. The currents of the feedback DACs are derived from the bandgap, wich includes the same type of resistors. The current defines the voltage drop across R_{sense}, obtaining an accurate compensation of the Hall sensitivity.

The additional chopping of the first integrator is combined with the spinning-current Hall effect by the input switches to reduce flicker noise and offsets.

To achieve both low noise and high stability in state-of-the-art higher-order CT-ΔΣ-ADCs, tuning of the time constants in the ΔΣ-loops is usually required due to the large temperature drift and the technology spread of integrated devices. In this work, a new compensation method with a bandgap-based on-chip relaxation oscillator solves this problem by using the same type of resistors and capacitors in the CT-ΔΣ-ADCs and in the bandgap-driven oscillator (Fig. 16.6.2). Thus, no frequency adjustment and no extra pins for an external crystal are needed. If required, synchronization to an off-chip system frequency may be done in the digital domain, instead of tuning the G_m-*C* or *RC* structures.

A simple 1st-order chopped CT-ΔΣ-ADC is used to measure on-chip temperature T and mechanical stress σ. The reference voltage across its sense resistor is again a replica derived from the bandgap, thus ensuring high accuracy.

The mechanical stress drift caused by the package shifts the magnetic sensitivity of Hall sensors by a few per cent due to piezoresistive and piezo-Hall effects [4]. This shift is significantly reduced by a new bias method, which uses two perpendicular p-diffusion resistors in a bandgap replica circuit to define the bias current of the n-well Hall plates (Fig. 16.6.4). For common {100} silicon this type of resistor has the smallest in-plane coefficient of piezoresistivity, $(\pi_{11} + \pi_{12})/2$ = 2.75%/GPa, when compared to n-polysilicon resistors or n-diffusion resistors, which have -24.4%/GPa. Yet the mere piezo-Hall coefficient P_{12} = 42%/GPa for in-plane stress leads to life-time sensitivity shifts of 2% for stress drifts of 25MPa. The new stress sensor principle is based on the different stress coefficients of n- and p-resistors: the p-type Hall bias current is mirrored onto two perpendicular n-diffusion resistors, which yields a notably stress-dependent voltage. The difference to a bandgap-based reference voltage of suitable temperature dependence and small stress drift by using vertical pnp-transistors [3] is proportional to mechanical stress. After conversion of both the T and σ signals by the second ADC, all input data for a fully digital compensation of the package-induced sensitivity drift are provided.

The IC is fabricated in 0.6μm BiCMOS technology and uses 6mm (Fig. 16.6.7). Measurements show low noise versus temperature-and-inupt-magnetic-field without spurious noise peaks (Fig. 16.6.5). The CT-ΔΣ-ADC achieves a DR of 90dB within 4kHz because of the additional digital tracking loop and range switching. The ratio of magnetic-offset-drift to bandwidth is four times better than reported in [1], and the temperature range is much wider too.

The new bias concept and stress sensor provide a signal for digital compensation of package-induced magnetic sensitivity drift that reduces the drift by at least 2 to 3 times. This stress compensation principle is also applicable to stable bandgap references and temperature sensors.

References:

[1] van der Meer, et al, "A Fully Integrated CMOS Hall Sensor with a 3.65μT 3σ Offset for Compass Applications," *ISSCC Dig. Tech. Papers*, pp. 246–247, Feb., 2005.

[2] O. Bajdechi and J.H Huijsing, "A 1.8-V ΔΣ Modulator Interface for an Electret Microphone with On-Chip Reference," *IEEE J. Solid-State Circuits*, vol. 37, pp. 279-285, Mar., 2002.

[3] F. Fruett, G.C.M Meijer and A.Bakker, "Minimization of the Mechanical-Stress-Induced Inaccuracy in Bandgap Voltage References," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1288-1291, Jul., 2003.

[4] U. Ausserlechner, M. Motz and M.Holliber, "Drift of Magnetic Sensitivity of Smart Hall Sensors Due to Moisture Absorbed by the IC-Package," *Proc. IEEE Sensors*, vol. 1, pp. 455-458, Oct. 2004.

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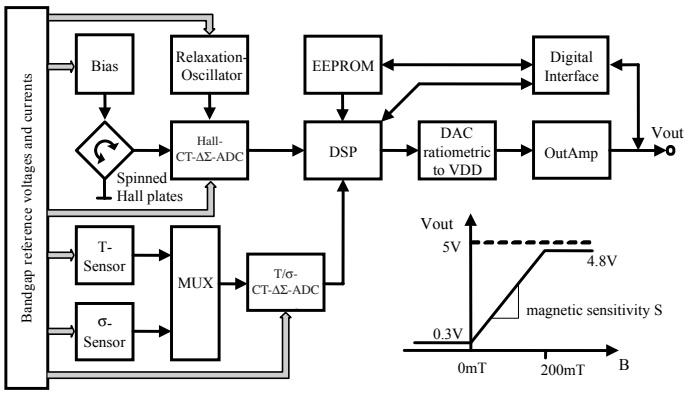

Figure 16.6.1: Hall sensor architecture.

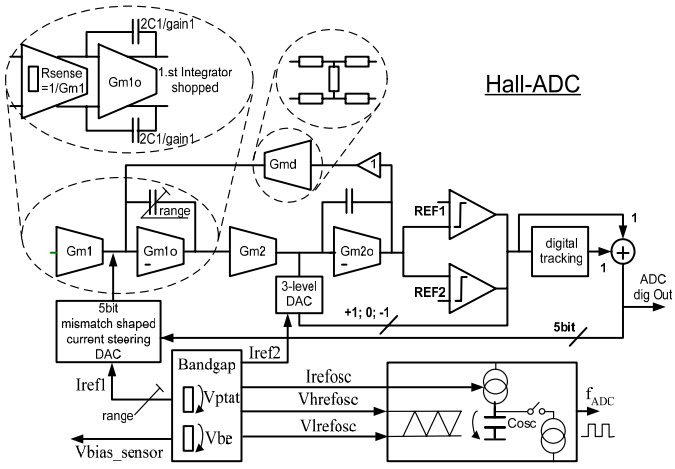

Figure 16.6.2: Chopped 3rd-order continuous-time multibit ΔΣ-ADC including digital tracking and loop compensation with the relaxation oscillator.

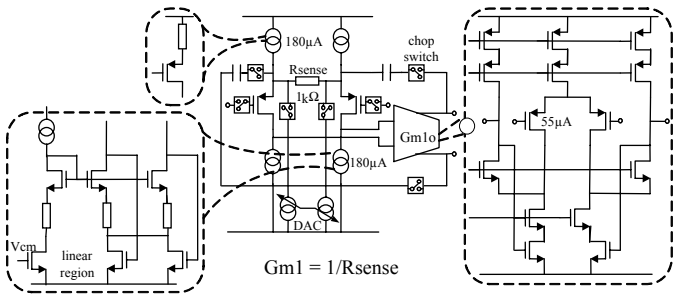

Figure 16.6.3: Chopped resistor-based Gm-C integrator.

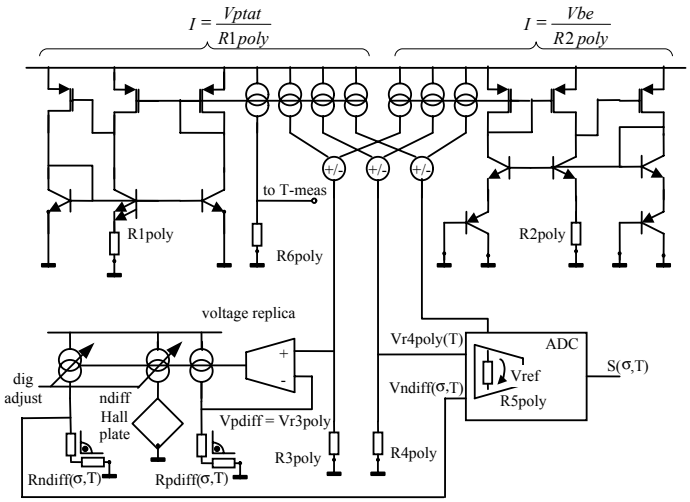

Figure 16.6.4: Stress-ADC input and stress robust bias for Hall sensor.

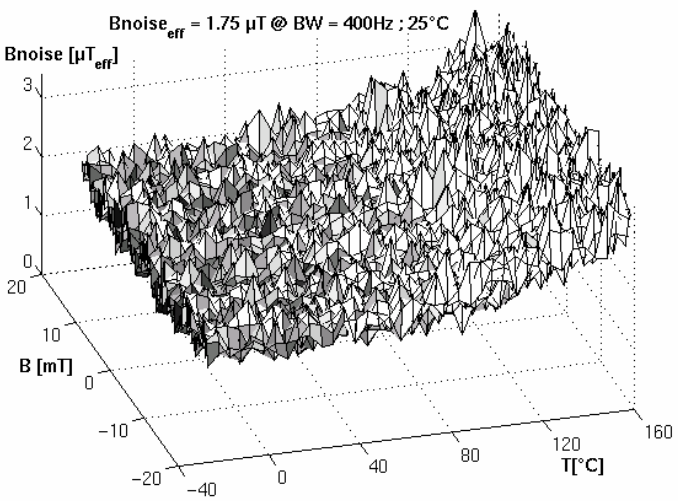

Figure 16.6.5: Measured noise of Hall-CT-ΔΣ-ADC versus temperature-and-input-magnetic-field.

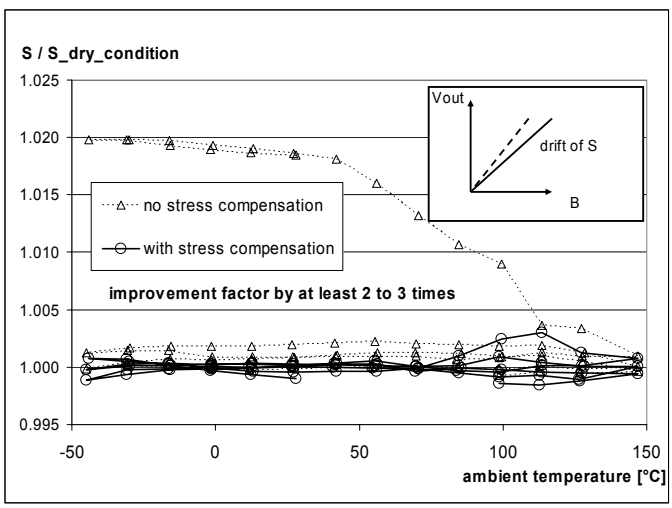

Figure 16.6.6: Drift of magnetic sensitivity S during thermal cycles (caused by changing package stress)

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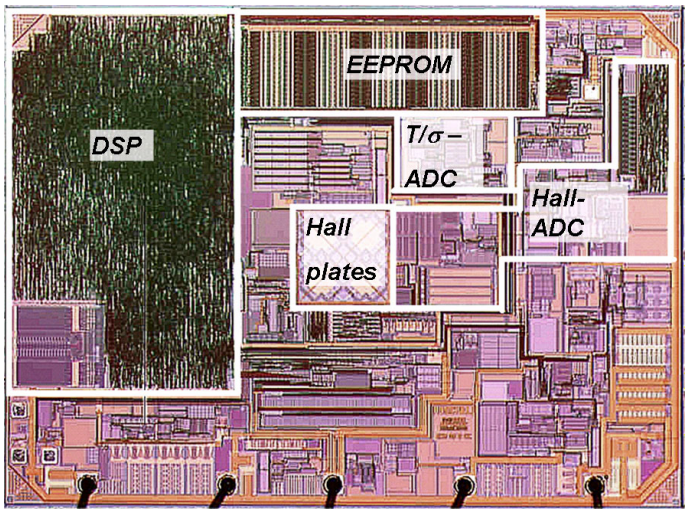

Figure 16.6.7: Chip micrograph of Hall sensor.

